Nano-laminate vs. Direct Deposition of High Permittivity Gadolinium Scandate on Silicon by High Pressure Sputtering

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In this work we use the high pressure sputtering technique to deposit the high permittivity dielectric gadolinium scandate on silicon substrates. This nonconventional deposition technique prevents substrate damage and allows for growth of ternary compounds with controlled composition. Two different approaches were assessed: the first one consists in depositing the material directly from a stoichiometric $GdScO_3$ target; in the second one, we anneal a nano-laminate of <0.5 nm thick Gd_2O_3 and Sc_2O_3 films in order to control the composition of the scandate. Metal-insulator-semiconductor capacitors were fabricated with platinum gates for electrical characterization. Accordingly, we grow a Gd-rich $Gd_{2-x}Sc_xO_3$ film that, in spite of higher leakage currents, presents a better effective relative permittivity of 21 and lower density of defects.

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I. INTRODUCTION

Gadolinium scandate competes with other oxides for replacing Hf-based high permittivity dielectrics in metal-insulator-semiconductor field effect transistors (MISFETs) [1,2,3,4,5]. This material could also be applied on high mobility substrates for high frequency applications [6]. Its main advantages over HfO_2 are that $GdScO_3$ remains amorphous and stable up to 1000 °C in contact with Si [7], showing a relative permittivity of 20-30 [8]. HfO_2 presents a low crystallization temperature (around 500 °C) [9], so a mixture of this oxide with SiON is used to keep the dielectric amorphous. However, this comes at the expense of lower relative dielectric constants (for example, 11 for $HfSiO_4$ [10]).

In the microelectronic industry, atomic layer deposition (ALD) predominates over other deposition techniques for high permittivity materials because of many reasons: thickness control, conformal growth, uniformity, reproducibility, interface control, scalability, etc [11,12]. Its main disadvantage is the moderately high deposition temperatures (300-500 ºC), used in order to avoid chlorine or carbon contamination from precursors. These temperatures tend to oxidize Si surface. On the other hand, physical vapor deposition based techniques provide simpler processes with low-cost of ownership. Particularly, high pressure sputtering (HPS) uses high purity targets with inert sputtering gases, so film contamination is expected to be low. Depositions are performed at low temperatures and pressures in the 100 Pa range, three orders of magnitude over conventional sputtering systems [13,14]. The sputtered atoms emitted from the target collide with the gas medium, lose their energy and thermalize within a short distance

(0.1–0.3 cm) [15,16]. This thermalization length is significantly shorter than the target-substrate distance (in our system 2.5 cm), so the particles reach the substrate by a pure diffusion process, preventing substrate damage. These lower deposition temperatures also minimize the undesirable SiO_x regrowth between the high permittivity material and the Si substrate, reducing the minimum equivalent oxide thickness (EOT) achievable. Conformability is also expected to improve with respect to conventional sputtering due to the short thermalization lengths.

This work compares gadolinium scandate deposited by HPS from a $GdScO_3$ target and the one obtained from a nano-laminate of <0.5 nm Sc_2O_3 and Gd_2O_3 layers, using in all cases high purity targets. The use of two different targets to deposit the nano-laminate allowed us to control the composition of the ternary $Gd_{2-x}Sc_xO_3$ through the thicknesses of the layers of the binary oxides. In fact, our purpose was to obtain Gd-rich $Gd_{2-x}Sc_xO_3$ because of two reasons: it presents higher relative permittivity than other compositions [17] and Gd_2O_3 presents better stability with Si than Sc_2O_3 [18]. For the electrical characterization, metal-insulator-semiconductor (MIS) capacitors were fabricated. With both kinds of dielectrics, we used Pt as the gate metal to avoid any reaction with the insulator layer and thus to measure the gadolinium scandate bare properties.

II. EXPERIMENTAL DETAILS

Dielectric deposition was performed on n-Si (100) wafers with a resistivity of 200-1000 Ω cm to measure the infrared absorption spectra of scandate films through the

Fourier transform infrared spectroscopy (FTIR) technique. A *Nicolet Magna-IR 750 series II* was used to get the infrared spectra in the 400-4000 cm^{-1} range. Reference Si spectrum was recorded after the immersion of the wafer in a diluted HF solution for 30 s to remove native SiO_2. X-ray photoemission spectroscopy (XPS) was measured in these samples by a *VG Escalab 200R* spectrometer equipped with a Mg K_α X-ray source ($h\nu$ = 1253.6 eV), powered at 120 W.

For MIS fabrication, n-Si (100) wafers with a resistivity of 1.5-5.0 Ω cm were used. Before dielectric deposition, a 200 µm SiO_x film was grown by e-beam evaporation and then, square windows were opened with sizes from 30×30 to 700×700 μm^2. This field oxide works as the electrical isolation between devices. Si surface was then prepared using a standard RCA (*Radio Corporation of America*) clean [19]. The sample was dipped in a 1:50 solution of HF for 30 s to remove native SiO_2, just before its introduction into the HPS system. After that, gadolinium scandate was deposited in a pure Ar atmosphere, at 100 Pa and 40 W of radiofrequency power. As stated in the introduction, gadolinium scandate deposition was carried out by two different methods. In the first one, ~7 nm thick $GdScO_3$ was grown from a stoichiometric and high purity target of this material. In the second method, <0.5 nm thick Sc_2O_3 and Gd_2O_3 layers were alternated up to a thickness of ~7 nm. For MIS fabrication, 50 nm of Pt were e-beam evaporated on the gadolinium scandate and lifted off by standard lithography. A 100 nm Ti/300 nm Al stack was evaporated on the backside of the wafer as the substrate contact. Finally, the devices were annealed in forming gas (FGA process) for 20 min at 300 and 450 °C. These low temperature annealings in forming gas are commonly used as one of the final steps of microchip fabrication to achieve interface trap passivation [20].

Moreover, back end of line limits annealing temperatures to 450 – 500 °C [21]. Admittance at 100 kHz and leakage current were measured with an *Agilent 4294A* impedance analyzer and a *Keithley 2636A* system respectively. EOTs were extracted by analyzing capacitance vs. voltage curves by means of the Hauser algorithm [22], which takes into account quantum-mechanical effects.

After electrical characterization the devices were studied through transmission electron microscopy (TEM). Samples were milled by a focused ion beam by means of the *ex-situ* lift out technique and were observed at 200 keV in a *Tecnai T20* microscope from *FEI*.

III. RESULTS AND DISCUSSION

We start with the analysis of the insulator/Si interface through the FTIR spectra of the samples. FTIR spectra are represented in Fig. 1 after subtraction of the Si wafer signal and they are shifted in the absorbance axis for the sake of clarity. Silicon oxide presents a Si-O transverse optical (TO) stretching vibration band centered at around 1077 cm^{-1} [23,24]. Fig. 1(a) shows this Si-O bands for the different ~7 nm dielectric films deposited on silicon, including the binary oxides Sc_2O_3 and Gd_2O_3, and the ternary $Gd_{2-x}Sc_xO_3$ deposited by the two different methods. Miyasaki et al. showed that the area of this band is proportional to the SiO_2 thickness [25], so the area of this peak between ~950 cm^{-1} and ~1020 cm^{-1} can be used as a qualitative estimation of the SiO_x interface layer thickness [26]. The shift towards lower wavenumber with respect to the ideal SiO_2 band is related

to the fact that the interface consists of Si suboxide and/or a stressed interfacial layer [23]. The bands that appear at ~820 and ~910 cm^{-1} are attributed to the correction of spectra with Si substrate and have been observed in previous works [18,27,28].

In Fig. 1(a), it can be seen that gadolinium scandate deposited from the stoichiometric target ($GdScO_3$) presents a SiO_x interface thicker than the nano-laminate (Gd_2O_3 + Sc_2O_3) and comparable with that of the Sc_2O_3. However, both Gd_2O_3 and the nano-laminate show a very thin, if any, SiO_x interface. FTIR thus indicate that Gd_2O_3 and the nano-laminated ternary system are more stable in contact with Si and that their interface oxide is thinner. As we will see, this is one of the reasons why the EOT obtained with this method is lower than using the stoichiometric target. On the other hand, Fig. 1(b) shows that, in the case of the $GdScO_3$, the FGA does not affect the amount of Si-O bonds, since their absorption does not change after the annealings at 300 and 450 °C. Thus, it can be concluded that no SiO_x growths during the annealings.

In order to analyze the composition of the grown films, XPS survey spectra were acquired and are shown in Fig. 2(a). The C 1s peak at a binding energy (BE) of 284.8 eV can be clearly seen in the survey scans. This adventitious carbon was the only contamination observed. Nevertheless, this kind of contamination could be due to the transport of the sample from the laboratory to the XPS system. For the binary oxides, although both targets (Gd_2O_3 and Sc_2O_3) were working during deposition, the Sc_2O_3 only displays the Sc 2p doublet, while the Gd_2O_3, the Gd 4d and 3d doublets. This indicates that the growth of the binary oxides is not contaminated by the other target although both are being sputtered during deposition. This is due to the small thermalization length, the

main advantage of HPS over conventional sputtering. Sc 2p doublet and Gd $3d_{5/2}$ peak can be observed in high resolution in Fig. 2(b). The areas of these curves provide the composition of the films. Quantitative XPS data indicate that both grown binaries are stoichiometric [18,29]. On the other hand, the composition calculated for the ternary oxide obtained from the nano-laminate is $Gd_{1.8}Sc_{0.2}O_3$ [28]. This way, the ternary oxide is Gd-rich, as we were aiming. Regarding the composition of the ternary grown from the stoichiometric target, the Sc/(Sc + Gd) atomic ratio obtained is around 0.5-0.6, which implies that the Sc content is slightly larger than that of Gd. This effect means that there is a preferential sputtering of Sc over Gd, a fact not surprising since its atomic mass is around 45 g mol^{-1}, which contrast with that of Gd around 157 g mol^{-1}. We will see later that the Gd-rich ternary compound shows better electric properties in terms of permittivity than the Sc-rich counterpart, as in ref. 17.

Fig. 3 depicts cross-sectional TEM images of the MIS devices after the annealings. From them, their thicknesses and structures can be approximately measured. Fig. 3(a) shows no appreciable SiO_x interface between the dielectric and the Si for the ternary system obtained from the two binary targets. Besides, no multi-layer structure can be observed inside this layer, implying that the FGA has achieved the intermixing of the films, as desired. A slight contrast within the layer may indicate that the interfacial SiO_x has diffused through the dielectric layer, forming a ~4 nm thick silicate in the proximity of the Si substrate. The two-layer structure was deduced according to images of the sample in back scattering electron mode (not shown) and the electron-dispersive X-ray (EDX), acquired during electron microscopy and shown in Fig. 4. Fig. 3(b) shows a 1.8 nm thick SiO_x for the ternary deposited from the stoichiometric $GdScO_3$ target. For both

kinds of deposition, the Pt gates do not react with the underlying dielectric. Fig. 4(a) and (b) plot the EDX sweeps following the white lines drawn at the right hand sides of Fig. 3(a) and (b), respectively. EDX shows the presence of diffused Si clearly within the $Gd_{1.8}Sc_{0.2}O_3$ film. However, we will see that, according to the electrical measurements, the formation of the silicate does not compromise effective permittivity.

On the other hand, Fig. 4(b) suggests that this silicon diffusion is smaller for the stoichiometric $GdScO_3$. The resulting stack in this case is thus a Sc-Gd-doped SiO_x with Sc-rich $GdScO_3$ on top. In the TEM image of Fig. 3(b), a slight contrast can be observed inside the $GdScO_3$ film. It could be caused by a change in the phase or in the composition. However, the TEM image does not show a pattern that could suggest a change in crystallinity EDX, while results in Fig. 4(b) do not suggest any change in composition. Although some Pt could be diffusing inside the dielectric, this does not affect strongly the electrical characteristics. The 1.8 nm thick SiO_x interface also explains the larger area of the peak corresponding to the Si-O bond in FTIR measurements (Fig. 2).

The high frequency capacitance vs. gate voltage (C_{HF}-V_G) curves of the MIS devices are plotted in Fig. 5. For the dielectric deposited from the $GdScO_3$ target, Fig. 5(b), the annealings do not change significantly the capacitance, so the effective relative permittivity of the dielectric stack (including the interfacial SiO_x) remains approximately at 10. In TEM and EDX discussions (Fig. 3 and 4), it was observed that a 1.8 nm thick SiO_x interface layer was developed between the $GdScO_3$ and the Si. This SiO_x interface must grow during ternary deposition. It remains with the same thickness after the FGAs,

so the ternary compound shows a good stability, at least up to 450 °C. Assuming a relative permittivity of 3.9 for this SiO_x layer, then the relative permittivity obtained for the gadolinium scandate is around 24, which agrees with the permittivity of the bulk material [8]. On the other hand, the C_{HF} in accumulation of the nano-laminate, shown in Fig. 5(a), follows a completely different trend: it increases slightly after FGA at 300ºC and doubles after the annealing at 450 °C. This means a dramatic decrease of the EOT down to 1.3 nm, and an increase in the effective permittivity of the whole stack ($Gd_{2-x}Sc_xO_3$ and its silicate) up to 21. The trends of the EOT value in all studied materials are summarized in Fig. 6. The strong decrease in the EOT is only observed for the scandate obtained from the nano-laminate. The nano-laminate needs to be annealed in order to produce the Sc_2O_3 and Gd_2O_3 intermixing, and only then the $GdScO_3$ permittivity is achieved. The EOT of Sc_2O_3 increases significantly when annealing at 300ºC, probably due to the regrowth of SiO_x interface. For Gd_2O_3 and the $GdScO_3$ obtained from the stoichiometric target, the SiO_x shows no regrowth after the annealings, implying that their stability is higher.

The increase in the permittivity of the $Gd_{2-x}Sc_xO_3$ obtained from the nanolaminate points to the actual formation of the ternary system after annealing at 450 ºC. Ref. 17 reported that Gd-rich $Gd_{2-x}Sc_xO_3$ presents higher dielectric constant than the stoichiometric ternary oxide. The increase of the permittivity with the mixing of both oxides is related to the appearance of Gd-Sc bonds that change the molecular polarizability of the compound. The polarizability and the dielectric constant are related through the Clausius-Mossotti equation [30].

The leakage current was evaluated for both kinds of ternary dielectrics and the results are displayed in Fig. 7. The leakage current increases for the $Gd_{2-x}Sc_xO_3$ up to 1 A cm^{-2} (at 1.5 V) accompanying the decrease in the EOT. This is another indication of a Si-rich silicate formation at the interface (that would present a bandgap lower than the SiO_x). For the dielectric deposited from the $GdScO_3$ target, the leakage curves are similar for the three conditions studied, showing only a very slight increase with FGAs. This is probably due to the fact that this current is actually limited by the high bandgap 1.8 nm thick SiO_x that remains unaffected by the FGAs. In any case, for these films the leakage remains under 10^{-4} A cm^{-2} and 1 A cm^{-2} at 1.5 V, which are good values for 2.5 nm and 1.3 nm EOT respectively [31].

In other to assess the quality of the scandate films, C_{HF}-V_G hysteresis curves are shown in Fig. 8, measured starting from accumulation. The loop can be due to trapping centers in the oxide, which can trap or emit a carrier depending on gate voltage polarity. Another possibility is the presence of charges within the oxide that move with gate voltage until they become fixed within the oxide matrix. Directly deposited $GdScO_3$ presents a high hysteresis loop of 0.49 V. In this case this value indicates a high density of trapped charge within the bulk dielectric. In contrast, the hysteresis of the ternary oxide obtained from the nano-laminate is around 55 mV. This means a low amount of bulk traps within the GdScSiO, and this value is low enough for the next generation of gate insulators [31,32].

Finally, the density of interface defects D_{it} was estimated by the conductance method [20] at 100 kHz. The dielectric deposited directly from the stoichiometric target has a D_{it}

slightly higher than the ternary system obtained from the nano-laminate (8×10^{11} compared to 6×10^{11} eV^{-1} cm^{-2}, respectively). These values are obtained after the passivation of the dangling bonds by the FGAs. Thus, we find again that a defective SiO_x is present at the interface between the ternary oxide and the Si, which agrees with hysteresis results. The D_{it} in the case of the ternary system obtained from the nano-laminate does not differ too much from the value obtained from ALD [4]. This means that the FGAs passivate effectively the Gd and Sc silicate present between the Gd-rich $Gd_{2-x}Sc_xO_3$ and the Si. The value of D_{it} and the hysteresis of the capacitance curves show that the 1.8 nm thick SiO_x between the Si and the ternary oxide obtained from the stoichiometric target is highly defective, even after the FGAs. However, the deposited nano-laminate, mixes after the FGA to give a Gd-rich scandate film over a Gd and Sc silicate with higher quality than the interface SiO_x.

IV. SUMMARY AND CONCLUSIONS

Gadolinium scandate was deposited by HPS through two different processes: sputtering of a stoichiometric $GdScO_3$ target or deposition of a nano-laminate of Sc_2O_3 and Gd_2O_3 films. The deposition of the nano-laminate let us control the composition of the film. The $GdScO_3$ obtained from the stoichiometric target is slightly Sc-rich and presents a 1.8 nm Gd and Sc doped SiO_x interface. This SiO_x is highly defective and its low permittivity limits the lowest EOT achievable, although it maintains a low leakage current. However, the latter approach permits obtaining, after an FGA at 450 °C, Gd-rich $Gd_{2-x}Sc_xO_3$. This Gd-rich ternary compound presents Si diffusion close to the dielectric-

Si interface with very low density of interface and slow defects. Besides, the dielectric stack presents an effective relative permittivity of 21 that would be adequate to substitute Hf-based dielectrics in next generations MISFETs.

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Figure Captions

Fig. 1. (a) FTIR spectra of ~7 nm thick Sc_2O_3, Gd_2O_3, $GdScO_3$ (from the high purity and stoichiometric target) and $Gd_{2-x}Sc_xO_3$ (from the nano-laminate) as deposited. (b) Spectra of the $GdScO_3$ as deposited and after the FGA at 300 and 450 °C.

Fig. 2. (a) XPS survey spectra of the Sc_2O_3, Gd_2O_3, $GdScO_3$ and $Gd_{2-x}Sc_xO_3$ films. (b) Sc 2p doublet and Gd $3d_{5/2}$ peak in high resolution.

Fig. 3. (a) TEM image of the Pt gated MIS with the $Gd_{2\ x}Sc_xO_3$ dielectric deposited from the Sc_2O_3 and Gd_2O_3 targets. (b) Pt gated MIS with the dielectric deposited from the $GdScO_3$ target. Both images were taken from samples that were annealed twice: first at 300 °C (then the electrical characterization was performed), followed by annealing at 450 °C (and then the final electrical measurement). The white lines at the right hand side of the images follow the path of the EDX analysis. On them, the tags correspond to points of the EDX sweep in Fig. 4.

Fig. 4. Intensity of electron excited X-rays as a function of position in the MIS devices. In (a) the gadolinium scandate was obtained from the nano-laminate and in (b) the dielectric was deposited from a high purity target of $GdScO_3$.

Fig. 5. C_{HF}-V_G characteristics of the the Pt/$Gd_{2\ x}Sc_xO_3$/Si device (a) and Pt/$GdScO_3$/Si device (b).

Fig. 6. Evolution of the EOT with the FGA for the Sc_2O_3, Gd_2O_3, $GdScO_3$ and $Gd_{2-x}Sc_xO_3$ films.

Fig. 7. Leakage current density (J_G-V_G) of the Pt/$Gd_{2-x}Sc_xO_3$/Si MIS (a) and the Pt/$GdScO_3$/Si (b).

Fig. 8. C_{HF}-V_G hysteresis curves for Pt/$Gd_{2-x}Sc_xO_3$/Si (a) Pt/$GdScO_3$/Si devices (b).

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[32] S. Zafar, A. Kumar, E. Gusev, E. Cartier, Threshold voltage instabilities in High-k Gate dielectric stacks, Trans. on Dev. and Mat. 5 (2005) 45.

Figure 1

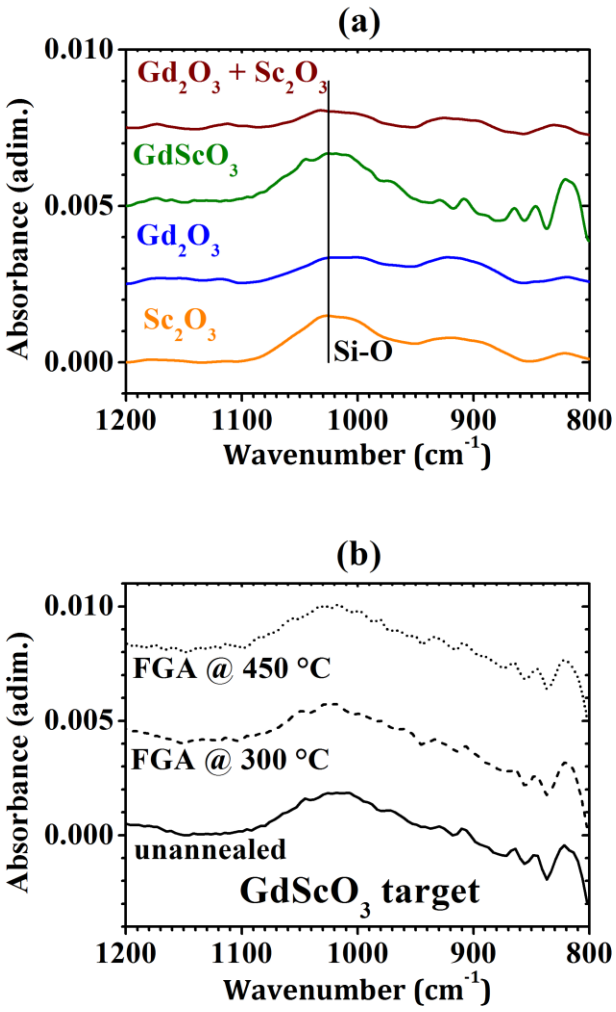

(a)
0.010
0.005
0.000
Absorbance (adim.)
Gd2O3 + Sc2O3
GdScO3
Gd2O3
Sc2O3
Si-O
1200
1100
1000
900
800
Wavenumber (cm-1)
(b)
0.010
0.005
0.000
Absorbance (adim.)
FGA @ 450 °C
FGA @ 300 °C
unannealed
GdScO3 target
1200
1100
1000
900
800
Wavenumber (cm-1)

Figure 2

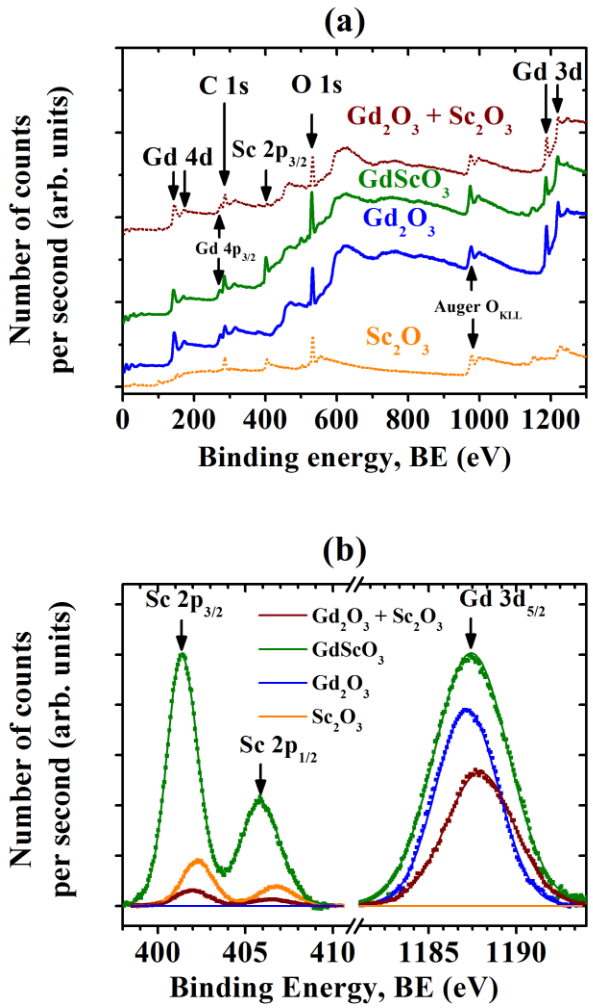

(a)
C 1s
O 1s
Gd 3d
Gd 4d
Sc 2p3/2
Gd2O3 + Sc2O3
GdScO3
Gd2O3
Gd 4p3/2
Auger OKLL
Sc2O3
Number of counts per second (arb. units)
0 200 400 600 800 1000 1200
Binding energy, BE (eV)
(b)
Sc 2p3/2
Gd 3d5/2
Gd2O3 + Sc2O3
GdScO3
Gd2O3
Sc2O3
Sc 2p1/2
Number of counts per second (arb. units)
400 405 410 1185 1190
Binding Energy, BE (eV)

Figure 3

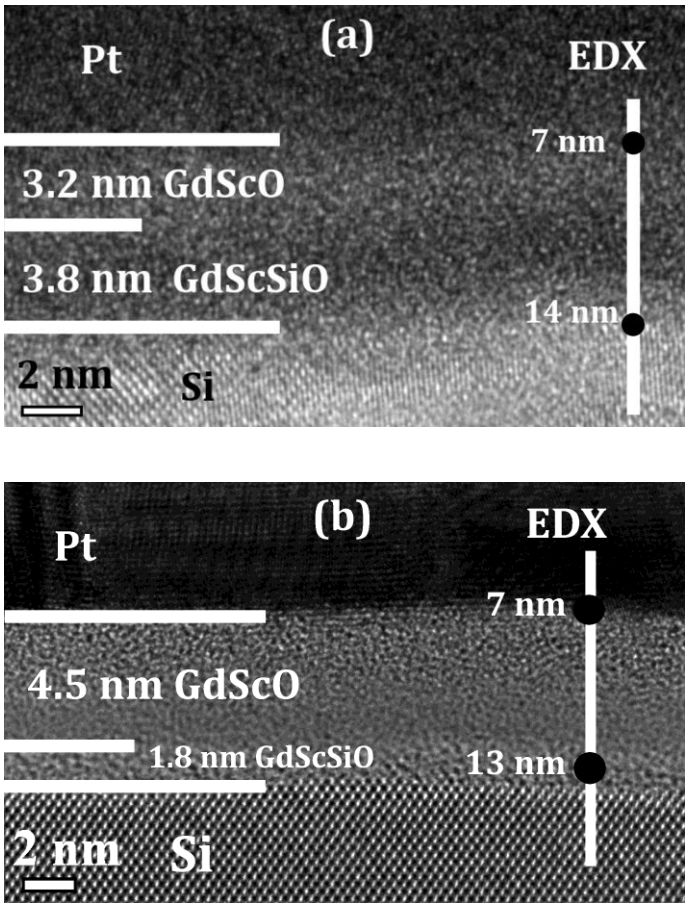

(a)
Pt
EDX
7 nm
3.2 nm GdScO
3.8 nm GdScSiO
14 nm
2 nm
Si
(b)
Pt
EDX
7 nm
4.5 nm GdScO
1.8 nm GdScSiO
13 nm
2 nm
Si

Figure 4

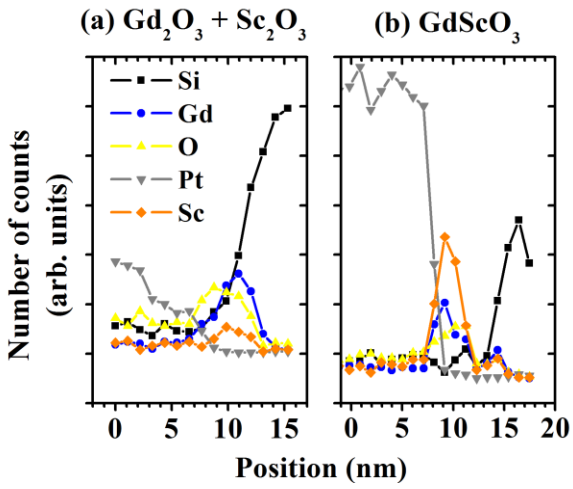

(a) Gd2O3 + Sc2O3
(b) GdScO3
Si
Gd
O
Pt
Sc
Number of counts
(arb. units)
0
5
10
15
0
5
10
15
20
Position (nm)

Figure 5

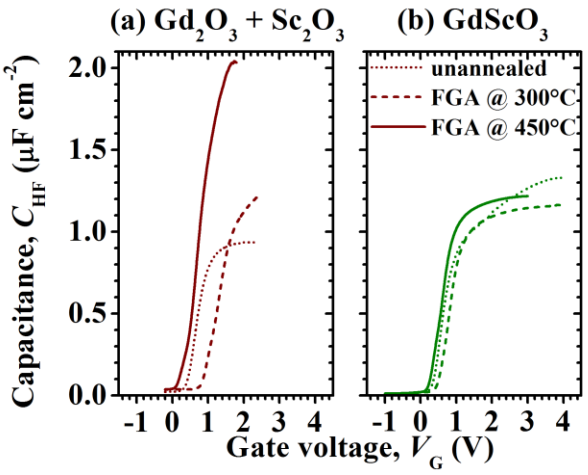

(a) Gd2O3 + Sc2O3
(b) GdScO3
unannealed
FGA @ 300°C
FGA @ 450°C
Capacitance, CHF (μF cm-2)
2.0
1.5
1.0
0.5
0.0
-1 0 1 2 3 4
-1 0 1 2 3 4
Gate voltage, VG (V)

Figure 6

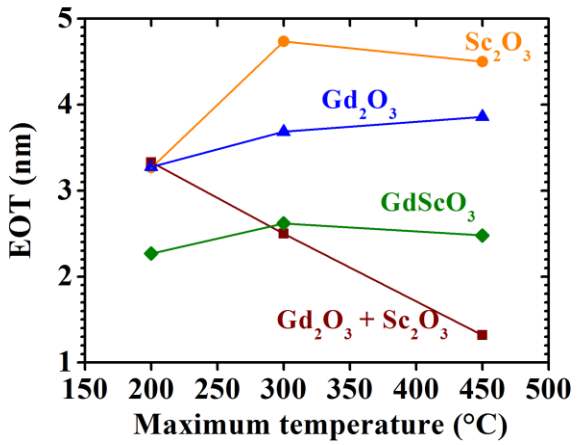

EOT (nm)
Maximum temperature (°C)
Sc2O3
Gd2O3
GdScO3
Gd2O3 + Sc2O3
1
2
3
4
5
150
200
250
300
350
400
450
500

Figure 7

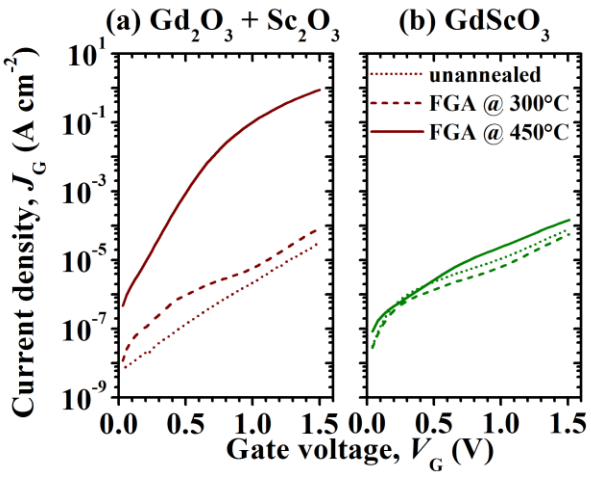
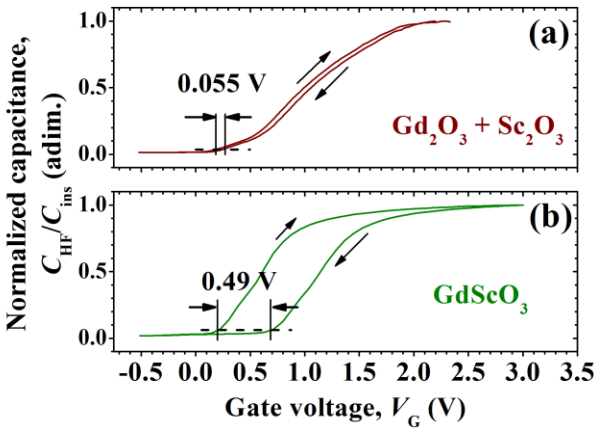

(a) Gd2O3 + Sc2O3
(b) GdScO3
unannealed
FGA @ 300°C
FGA @ 450°C
Current density, JG (A cm-2)
Gate voltage, VG (V)
10^1
10^-1
10^-3
10^-5
10^-7
10^-9
0.0
0.5
1.0
1.5

Figure 8


(a)
0.055 V
$Gd_2O_3 + Sc_2O_3$
(b)
0.49 V
$GdScO_3$
Normalized capacitance, C_{HF}/C_{ins} (adim.)
Gate voltage, V_G (V)
1.0
0.5
0.0
-0.5 0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5